What is claimed is:

1. A camouflaged interconnection scheme for interconnecting two spaced-apart implanted regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising:

a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions, the conducting channel being of said common conductivity type and bridging a region between said two spaced-apart regions; and

a second implanted region of opposite conductivity type in the integrated circuit or device, said second implanted region being disposed between said two spaced-apart implanted regions of common conductivity type and overlying said conducting channel.

2. The invention of claim 1 wherein said second implanted region overlying said conducting channel has a larger area, when viewed in a direction normal to a major surface of in the integrated circuit or device, than has said conducting channel.

3. The invention of claim 1 wherein said two spaced-apart implanted regions form source and/or drain contacts, respectively, of two separate field effect transistors (FETs).

4. The invention of claim 1 wherein the second implanted region is provided in said integrated circuit or device over regions having no conducting channels formed therein.

5. A camouflaged interconnection scheme for interconnecting a plurality of spaced-apart implanted regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising:

a plurality of interconnects each interconnecting selected implant regions of said plurality of spaced-apart implanted regions, each interconnect comprising a buried conducting channel

bridging a region between the selected implant regions; and

at least one implanted region of opposite conductivity type in the integrated circuit or device, the at least one implanted region of opposite conductivity type being disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects.

6. The invention of claim 5 wherein said at least one implanted region of opposite conductivity type has a larger area than a total area of a related at least one of said conducting channels, when viewed in a direction normal to a major surface of in the integrated circuit or device.

7. The invention of claim 5 wherein at least selected one of said spaced-apart implanted regions form source and/or drain contacts, respectively, of adjacent field effect transistors (FETs).

8. The invention of claim 5 wherein the second implanted region is provided in said integrated circuit or device over regions having no conducting channels formed therein.

9. A method of providing and camouflaging an interconnect between two adjacent implanted regions in an integrated circuit or device, the two adjacent implanted regions being of a common conductivity type, said method comprising:

implanting a first region of said common conductivity type, said first region being disposed between locations where said two adjacent implanted regions either have been or will be formed; and

implanting a second region of opposite conductivity type to said common conductivity type, said second region overlying at least said first region and having a concentration profile normal to a major surface of said integrated circuit or device with a concentration peak closer to said major surface of the semiconductor device than a concentration peak for the first implanted

region.

10. The method of claim 9, wherein said first region is implanted at a higher energy than is said second region.

11. The method of claim 9, wherein said second region is implanted before said first region is implanted.

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12. The method of claim 9, wherein said first region is implanted during the implantation of active regions associated with transistors formed in said integrated circuit or device.

13. The method of claim 12 wherein said active regions are source and/or drain regions and wherein said transistors are FET devices formed in said integrated circuit or device.

14. The method of claim 9, wherein the step of implanting a second region of opposite conductivity type to said common conductivity type includes implanting said second region in regions of said integrated circuit or device where interconnections between active regions could plausibly occur but do not occur.

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